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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448

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ON Semiconductor
Patent Administration Dept - MD A700
P.O. Box 62890
Phoenix, AZ 85082-2890

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/072,145	AVERETT ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 41 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the embodiment of figure 6 for the claimed limitation of "the polysilicon cap layer is aligned with each of the plurality of voids without completely overlying each of the plurality of voids", as recited in claim 41.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 40 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitation of "the matrix of pillars", as recited in claim 40, is unclear as to whether the matrix of pillars is the same matrix recited in claim 39, or a different element.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 34 and 38-41, as best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Lur et al. (5,640,041).

Lur et al. teach in figures 10 and 14 and related text an intermediary of a semiconductor device, comprising:

a semiconductor substrate 10 formed with a first recessed region having a lower surface depressed with respect to a major surface of the semiconductor substrate;

a pillar region (the regions which includes pillars 24) comprised of a plurality of pillars comprising a silicon dioxide dielectric material formed in the first recessed region and extending from the lower surface, wherein a plurality of voids (the rectangular area outside the boundaries of pillars 24) within the pillar region; and

a polysilicon cap layer 5 having a surface formed adjoining upper surfaces of the pillar region and overlying each of the plurality of pillars, wherein the surface of the polysilicon cap layer is aligned with each of the plurality of voids, and wherein sidewall surfaces of the plurality of pillars are devoid of the polysilicon cap layer, and wherein the

pillar region, the polysilicon cap layer and the void region are configured to form an isolation region having reduced substrate capacitance.

Regarding claims 39-41, Lur et al. teach in figure 10 and related text the pillar region comprises a matrix of pillars 24, wherein at least a portion of the matrix of pillars includes pillars having a generally rectangular shape, and wherein the polysilicon cap layer is aligned with each of the plurality of voids without completely overlying each of the plurality of voids.

Regarding claim 38, the claimed limitations of a pillar region comprises deposited silicon dioxide, these are process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 35-37 and 42, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al.

Regarding claim 35, Lur et al. teach substantially the entire claimed structure, as recited in claim 34, except explicitly stating that the polysilicon cap layer has a thickness of about 4,500 angstroms. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the polysilicon cap layer having a thickness of about 4,500 angstroms in prior art's device in order to reduce the size of the device.

Regarding claim 36, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recess the upper surfaces of the pillar region below the major surface of the semiconductor substrate, in prior art's device in order to adjust the characteristics of the device according to the requirements of the application in hand.

Regarding claim 37, Lur et al. do not state that the upper surfaces are recessed a distance of about 0.5 microns. It would have been obvious to a person of ordinary skill

in the art at the time the invention was made to form the upper surfaces recessed a distance of about 0.5 microns in prior art's device in order to adjust the characteristics of the device according to the requirements of the application in hand.

Regarding claim 42, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form pillar region extending a distance of about 4.5 micrometers from the lower surface of the first recessed region and has a dielectric constant of about 3.5 in prior art's device in order to reduce the size of the device and in order to adjust the characteristics of the device according to the requirements of the application in hand, respectively.

Response to Arguments

Applicant argues that "Lur does not show nor make obvious a polysilicon cap layer having a surface formed adjoining upper surfaces of the pillar region and overlying each of the plurality of pillars", because "Lur shows a structure wherein the polysilicon layer 5 does not overlie each of the plurality of pillars. Some of the pillars in Lur do not have any polysilicon layer 5 overlying them".

Applicant further argues that Lur does not teach "surface of the polysilicon cap layer to be aligned with each of the plurality of voids, because "Lur's polysilicon layer 5 is not aligned with each of the plurality of voids. Lur shows a polysilicon layer 5 which is deposited entirely over numerous voids and not aligned with each void".

Claim 34 calls for a pillar region comprised of a plurality of pillars wherein a polysilicon cap layer overlying each of the plurality of pillars. Two pillars are "plurality of pillars". Clearly, polysilicon cap 5 of Lur overlies two pillars. Therefore, Lur teaches a pillar region comprised of a plurality of pillars (two pillars) wherein a polysilicon cap layer overlying each of the plurality of pillars, as claimed.

Furthermore, since polysilicon cap 5 of Lur is located vertically above the entire number of the plurality of pillars, then polysilicon cap 5 of Lur overlies the entire number of the plurality of pillars.

Moreover, the claimed limitations of "a polysilicon cap layer having a surface formed adjoining upper surfaces of the pillar region and overlying each of the plurality of pillars" are unclear, for the following reasons. Figure 6 depicts plurality of polysilicon cap layers 175 spaced apart from each other, **and not one cap layer**. Furthermore, said "plurality of polysilicon cap layers 175" having a surface formed adjoining **only one** upper surface of the pillar region 60, and not adjoining plurality of upper surfaces of the pillar region. **There are no plurality of upper surfaces of the pillar region 60**. Regarding the phrase "overlying each of the plurality of pillars", it is unclear whether the polysilicon cap layer or the surface of the polysilicon cap layer overlies each of the plurality of pillars.

Regarding applicant's argument that Lur does not teach "surface of the polysilicon cap layer to be aligned with each of the plurality of voids", the surface of Lur's polysilicon layer 5 is the surface located around polysilicon layer 5, which includes

the right vertical surface, the top horizontal surface and the left vertical surface. As discussed above, plurality of voids means two voids. Clearly, the right vertical surface and the left vertical surface of polysilicon layer 5 are each vertically aligned with one void, so that the surface of polysilicon layer 5 is aligned with two voids. Therefore, Lur teaches the claimed limitation of "surface of the polysilicon cap layer to be aligned with each of the plurality of voids".

Note however, that the broad recitation of the claim does not require that the lower surface of the polysilicon cap layer is aligned with the top surface of each of the plurality of voids.

Although the claimed invention is anticipated by Lur, **the examiner agrees that Lur does not teach the limitations of a lower surface of the polysilicon cap layer to be aligned with a top surface of each of the plurality of voids.**

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
10/20/2009

/ORI NADAV/
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800